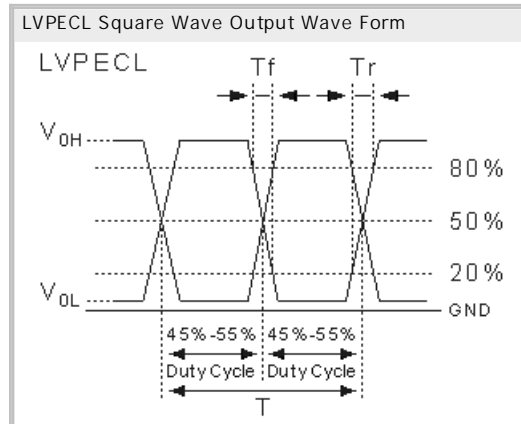
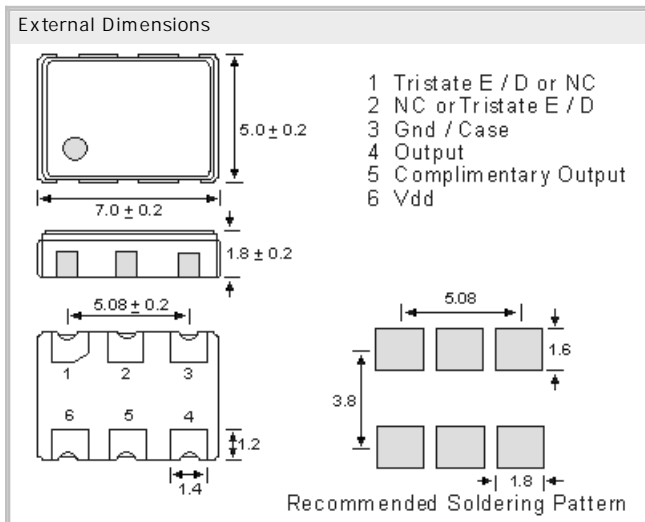


Clock Oscillator LVPECL Differential
CXO7050PF3.3-1/2, 3.3V, ultra low jitter

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1 or 2
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies



Specifications - Product No. G106250000CRCUPN00BB

Holder Type:	CXO7050PF3.3-1/2; 3.3V(Voltage code is "3.3"); Tri-State on pad 1 or 2
Frequency:	106.250000 MHz
Frequency Stability at 25°C:	± 50.0 ppm
Operating Temperature Range:	± 50.0 ppm over -20°C to +70°C (inclusive of 25°C tolerance, ± 10% input voltage variation, load change, aging, shock and vibration)
Storage Temperature:	-55°C to +150°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 5%
Maximum Supply Current (15pF load):	80.0 mA max.
Output Logic Levels:	High "1" Voh Vdd-1.025min., Termination: RL= 50 Ohm to (Vdd-2.0V) Low "0" Vol Vdd-1.620max., Termination: RL= 50 Ohm to (Vdd-2.0V)
Output Symmetry (Duty Cycle):	50% ± 5% max. @ Vdd-1.3V
Load:	RL= 50 Ohm for (Vdd-2.0V)
Rise/Fall Time:	0.4ns typical, 0.55ns max. @ 20% to 80% of PECL wave form
Start Up Time:	10 ms max.
Tri-state Function Pin 1 (or 2):	When Pin 1 (or 2) = 1, Output Enable When Pin 1 (or 2) (at 0.0V), Output High impedance, Disable current: 50µA max.
Phase Jitter (12 kHz to 20 MHz):	0.4 ps typ., 0.5 ps max., for 156.250MHz
Period Jitter, RMS, peak to peak:	(decoupling capacitor between Vdd and GND) for 156.250 MHz RMS: 3ps typ., 5ps max; peak to peak: 20ps typ; 30ps max.
Phase Noise (156.250 MHz):	-62dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -120dBc/Hz @ 1kHz -132dBc/Hz @ 10kHz, -130dBc/Hz @ 100kHz, -140dBc/Hz @ 1MHz
Input Static Discharge Protection:	2 kV (min.)
Aging:	< ± 3ppm max. for the first year
Reflow Condition:	260°C max for 10 sec.

GERMANY:

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