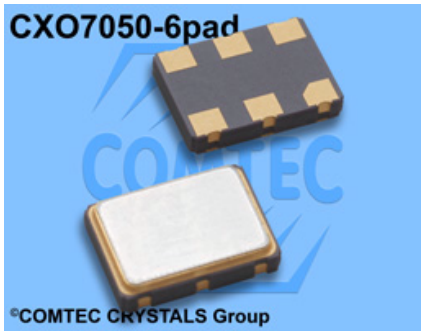
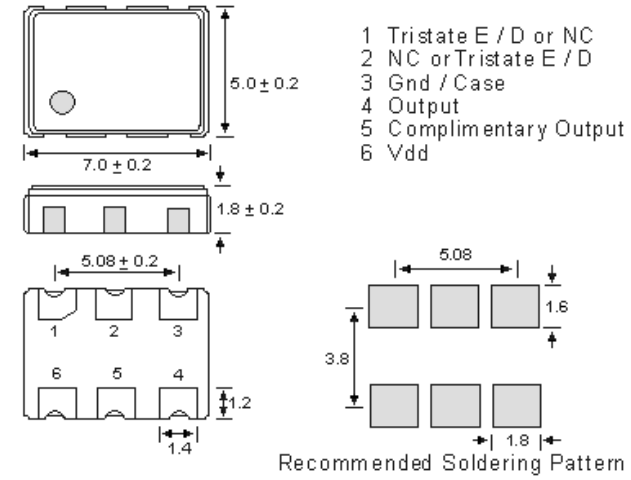


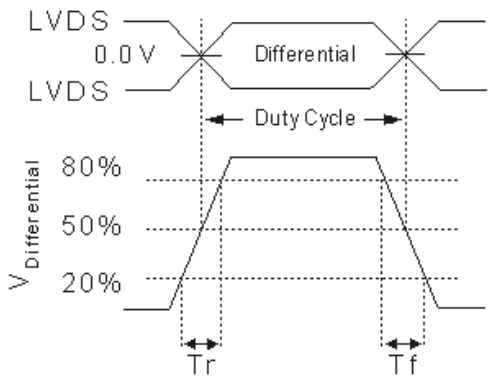
Differential LVDS Clock Oscillator
CXO7050DK3.3, 3.3V, 0.2pS Jitter

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- Femto second integrated phase jitter (0.2ps typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -142 dBc/Hz at 100 KHz offset)
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave

Differential LVDS Clock Oscillator CXO7050DK3.3



LVDS Square Wave Output Wave Form



Specifications

Holder Type:	Differential LVDS Clock Oscillator CXO7050DK3.3; 3.3V; Tri-State on pad 1
Frequency:	125.000000 MHz
Frequency Stability at 25°C:	± 50.0 ppm
Operating Temperature Range:	± 50.0 ppm over -20°C to +70°C (incusive of 25°C tolerance, ±10% input voltage variation, load change, aging, shock and vibration)
Storage Temperature:	-50°C to +100°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 5%
Maximum Supply Current (15pF load):	16.0 mA typ.
Output Swing:	350 mV min. (Vdd = +2.5V)
Output Logic Levels:	High "1" 1.43V typical; 1.6V max, RL=100 ohms.; Low "0" 0.9V min; 1.1V typical, RL=100 ohms
Output Symmetry (Duty Cycle):	50% ± 5%max. measured at 50% waveform
Load:	RL=100 Ω between output and complimentary output
Rise/Fall Time:	Tr = 0.2 ns. typ; 0.4 ns. max. 20% -> 80% of waveform Tf = 0.2 ns. typ; 0.4 ns. max. 80% -> 20% of waveform
Start Up Time:	5.0 ms typical; 10.0 ms typical;
Tri-state Function Pin 1:	If no connection or Vdd *70% min is applied: Output. Internal pull-up Oscillation disable time is 2µs max. If Vdd*30% max is applied: High impedance. 10µA typ., enable time 2ms max.
Phase Jitter (12 kHz to 20 MHz):	0.2 ps typical, 0.5 ps (max.)
Phase Noise (125 MHz):	-60dBc/Hz @ 10Hz, -90dBc/Hz @ 100Hz, -120dBc/Hz @ 1kHz -136dBc/Hz @ 10kHz, -142dBc/Hz @ 100kHz, -145dBc/Hz @ 1MHz, -148dBc/Hz @ 10MHz
Aging:	< ±3ppm max. for the first year
Reflow Condition:	260°C max for 10 sec.

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