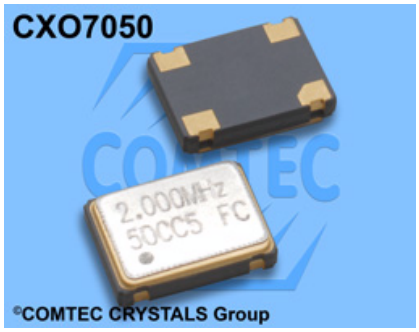
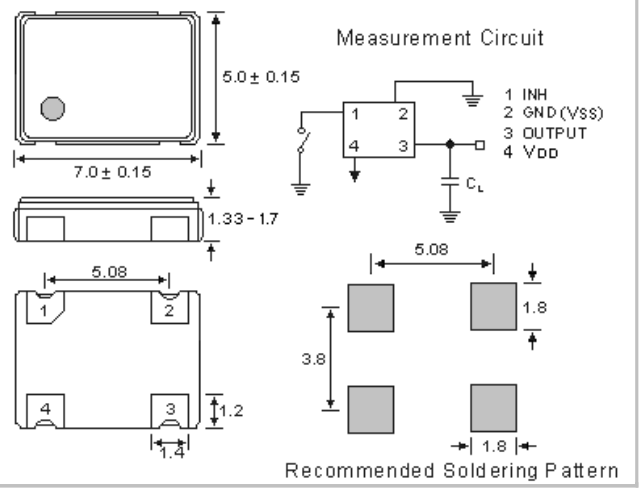


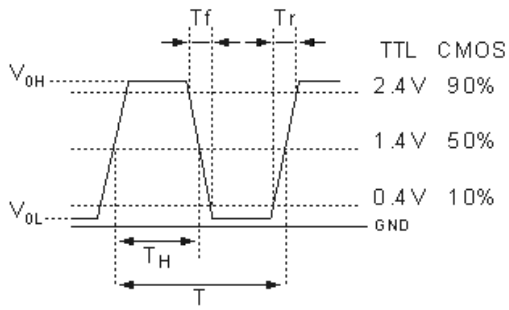

Crystal Clock Oscillator CXO7050T3.3
3.3V CMOS/TTL, Low cost

- SMD in ceramic case (7.0 x 5.0 x 1.7) mm
- Tri-State Enable / Disable
- CMOS/TTL Square Wave
- on Tape & Reel (Tape 16mm)
- RoHS conform; Lead-free product
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies

Crystal Clock Oscillator CXO7050T3.3 CMOS/TTL




CMOS/TTL Output Wave Form




## Specifications

| | |
|---|---|
| Holder Type: | Crystal Clock Oscillator CXO7050T3.3 3.3V CMOS/TTL |
| Frequency Range: | 312.0kHz ~ 160 MHz |
| Frequency Stability at 25°C: | ±20 to ±100 ppm |
| Operating Temperature Range: | -20°C to +70°C, -40°C to +85°C, (100ppm) -40°C to +105°C (Inclusive of 25°C tolerance, operating Temp., Supply Voltage, & Load, aging, shock and vibration) |
| Storage Temperature: | -50°C to +105°C |
| Power Supply Voltage (Vdd): | + 3.3V D.C. ± 5 % |
| Maximum Supply Current: | 5mA max. (25kHz ~ 1.5MHz) 8mA max. ( 1.5MHz ~ 20MHz)<br>15mA max. ( 20MHz ~ 50MHz) 35mA max. (50MHz ~ 200MHz) |
| Output Load: | 15pF CMOS (30pF and 50pF optional ) / 10LS TTL gates max. |
| Output Symmetry (Duty Cycle): | 40/60% (45/55% optional) |
| Output Voltage (V0H) (V0L): | 90% of Vdd min. / 10% of Vdd max. |
| Rise/Fall Time (10% to 90% Vdd): | 10 ns max. < 5 ns typical |
| Start Up Time: | 10 ms max. < 5 ms typical |
| Tri-state Function Pin 1: | Pin 1 = H or open.... Output active at pin 3<br>Pin 1 = L.... high impedance at pin 3 |
| Phase Jitter (12 kHz to 20 MHz): | < 1pS RMS |
| Aging: | < ±5ppm max. / year (max.) |
| Moisture sensitivity level: | MSL=1 per IPC/JEDEC J-STD-020 C |
| Reflow Condition: | 260°C max for 10 sec. |

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