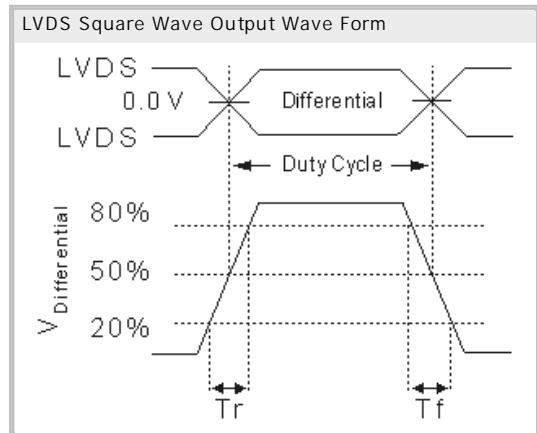
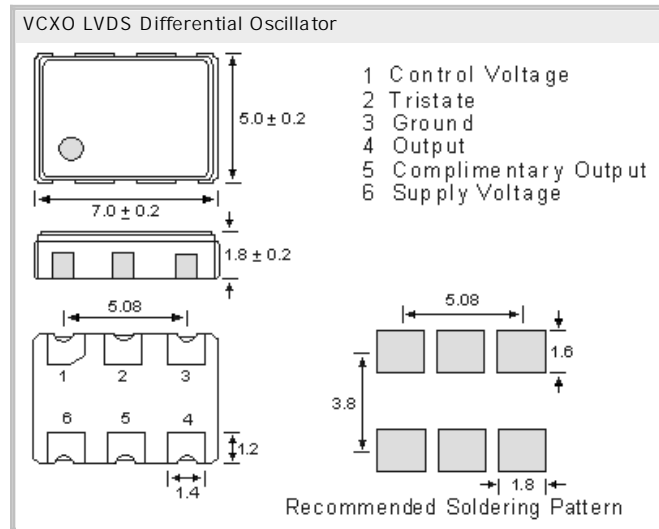


VCXO LVDS Differential Oscillator, VCXO7050DF3.3 3.3V, ultra low jitter

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- LVDS Square Wave Output Wave Form
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies



Specifications

Holder Type:	VCXO LVDS Differential Oscillator, CXO7050DF3.3 3.3V(Voltage code is "3.3"); Tri-State on pad 2
Frequency Range:	38.000 MHz to 640.000 MHz
Frequency Stability at 25°C:	± 20 to ± 100 ppm
Operating Temperature Range:	± 20 to ± 100 ppm, -20°C to +70°C, -40°C to +85°C
Frequency Deviation:	± 100ppm (typ.), ± 150ppm
Storage Temperature:	-55°C to +150°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 5%
Maximum Supply Current (15pF load):	38mA max.(38.00MHz ~ 100.00MHz); 40mA max.(100.01MHz ~ 320.00MHz); 45mA max.(320.01MHz ~ 640.00MHz)
Load:	RL= 50 from each output
Output Logic Levels:	High "1" Voh Vdd-1.025min., -0.95typ., -0.88max.; RL= 50 to (Vdd-2.0V) Low "0" Vol Vdd-1.810min., -1.70typ., -1.62max.; RL= 50 to (Vdd-2.0V)
Output Symmetry (Duty Cycle):	50% ± 5% max.@ Vdd-1.3V
Voltage Control:	1.65V DC Center / 0.3V to 3.0V Range
Rise/Fall Time:	0.2ns typical, 0.4ns max. @ 20% to 80% of LVDS wave form
Start Up Time:	5 ms max.
Tri-state Function Pin 2:	When Pin 2 = 1, Output Enable When Pin 2 (at 0.0V), Output High impedance, Disable current: 50µA max.
Phase Jitter (12 kHz to 20 MHz):	0.4 ps typ., 0.5 ps max., for 156.250MHz
Phase Noise (156.250 MHz):	-62dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -120dBc/Hz @ 1kHz -132dBc/Hz @ 10kHz, -128dBc/Hz @ 100kHz, -140dBc/Hz @ 1MHz
Aging:	< ± 3ppm max. for the first year
Input Impedance:	60 k (min.)
Reflow Condition:	260°C max for 10 sec.

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