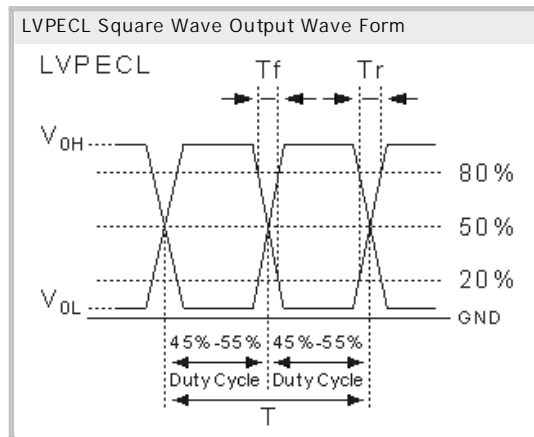
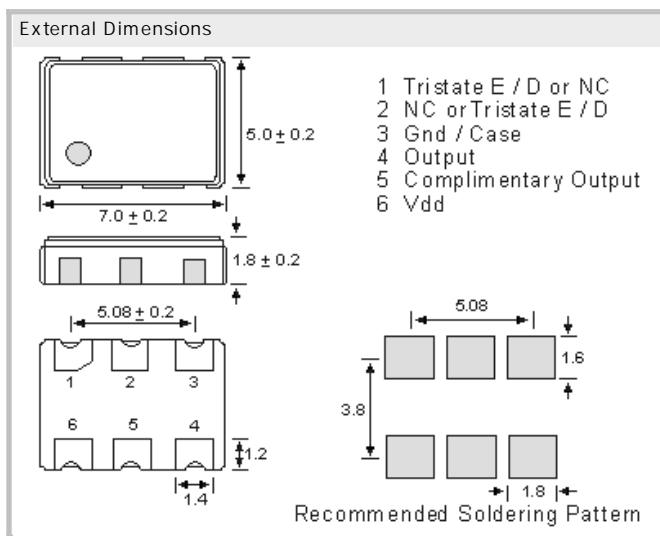


Differential LVPECL Clock Oscillator  
CXO7050PK 3.3, 3.3V, 200 fsec Jitter

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- Femto second integrated phase jitter (200 fs typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -144 dBc/Hz at 100 KHz offset)
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- High performance with surprisingly low price



## Specifications

|                                     |   |
|-------------------------------------|---|
| Holder Type:                        | CXO7050PK 3.3; 3.3V(Voltage code is "3.3"); Tri-State on pad 1  |
| Frequency Range:                    | 13.500 MHz ~ 220.000 MHz  |
| Frequency Stability at 25°C:        | ± 20 to ± 100 ppm   |
| Operating Temperature Range:        | -20°C to +70°C, -40°C to +85°C  |
| Storage Temperature:                | -55°C to +150°C   |
| Power Supply Voltage (Vdd):         | + 3.3V D.C. ± 5%  |
| Maximum Supply Current (15pF load): | 35mA typical 50mA max.  |
| Output Logic Levels:                | High "1" Voh Vdd-1.025V min., Vdd-0.95 V typical;<br>Vdd-0.88V max. Condition: RL= 50 Ohm to (Vdd-2.0V)<br>Low "0" Vol Vdd-1.810V min., Vdd-1.70 V typical;<br>Vdd-1.62V max. Condition: RL= 50 Ohm to (Vdd-2.0V) |
| Output Swing:                       | 595 mV min; 750 mV typical; 930 mV max.   |
| Output Symmetry (Duty Cycle):       | 50% ± 5% max. measured at 50% waveform  |
| Load:                               | RL= 50 Ohm into (Vdd-2.0V) or<br>Thevenin equivalent (terminating resistors required on all outputs).   |
| Rise/Fall Time:                     | 0.3ns typical, 0.5ns max. @ 20% to 80% of PECL wave form  |
| Start Up Time:                      | 3 ms typical; 10 ms max.  |
| Tri-state Function Pin 1 (or 2):    | If no connection or Vdd * 70% min is applied: Output. Internal pull-up<br>Oscillation disable time is 2ms max.<br>If Vdd* 30% max is applied: High impedance. 10µA typ., enable time 2ms max.                     |
| Phase Jitter (12 kHz to 20 MHz):    | 200 fs typical  |
| Phase Noise (62.5 MHz):             | -50dBc/Hz @ 10Hz, -82dBc/Hz @ 100Hz, -116dBc/Hz @ 1kHz<br>-138dBc/Hz @ 10kHz, -144dBc/Hz @ 100kHz, -149dBc/Hz @ 1MHz  |
| Aging:                              | < ± 3ppm max. for the first year  |
| Reflow Condition:                   | 260°C max for 10 sec.   |

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