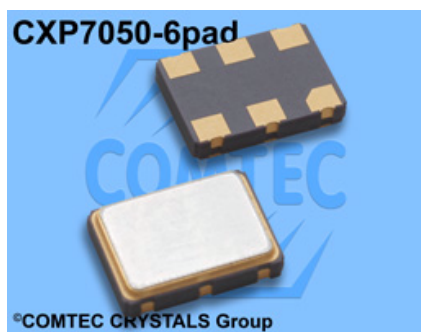
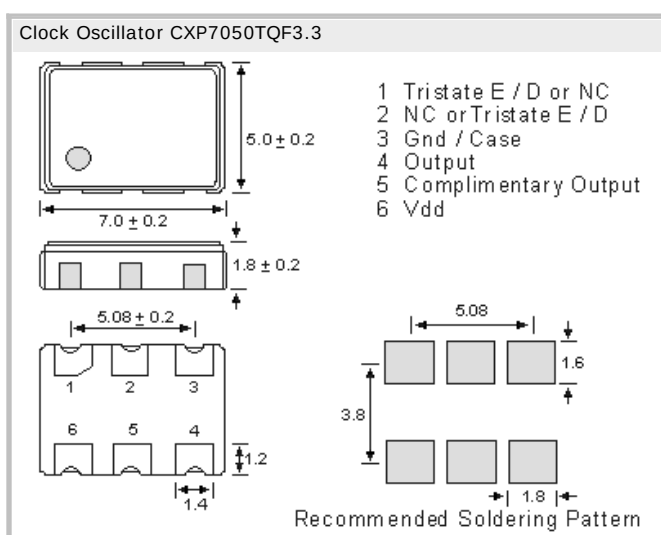


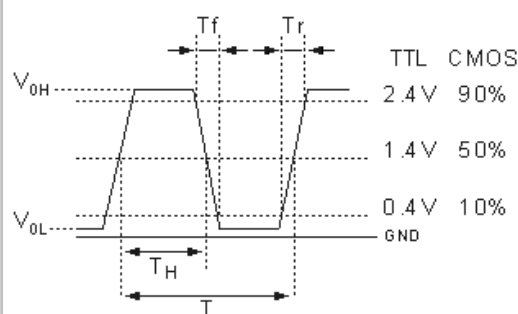


Clock Oscillator CXP7050TQF3.3
LVCMOS/LVTTL 3.3V; ultra low jitter, with PLL

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- LVCMOS/LVTTL Square Wave Output Wave Form
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product;
- on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies



CMOS Output Wave Form



Specifications

Holder Type:	CXP7050TQF3.3; 3.3V(Voltage code is "3.3"); Tri-State on pad 1
Frequency Range:	10 MHz to 245.0 MHz
Frequency Stability at 25°C:	±25 ppm, ±50 ppm
Operating Temperature Range:	±25 ppm, -40°C to +85°C / ±50 ppm, -40°C to +85°C
Storage Temperature:	- 55°C to +125°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 10%
Maximum Supply Current (15pF load):	10 MHz 17 mA typical, 150MHz 28 mA 10 MHz 17 mA typical, 150MHz 28 mA
Output Logic Levels:	High "1" 90% of Vdd-min, Low "0" 10% Vdd-max.,
Start Up Time:	10 ms max.
Output Symmetry (Duty Cycle):	50% ± 2% max. (measured at 50% Vdd)
Load:	15pF
Rise/Fall Time:	1.5ns typical; 3.0ns max. (10%Vdd<->90%Vdd, 15pF load)
Tri-state Function Pin 1 OE Control:	0.7% of Vdd min. or no connection to enable output. LVCMOS/LVTTL level. 0.3% of Vdd max.to disable output (high impedance). LVCMOS/LVTTL level.
Output Enable Time / Disable Time:	200 nS. Max. / 50 nS. Max.
Phase Jitter:	1.0 ps typ. (12 kHz to 20 MHz); < 100 fs (1.875 MHz to 20MHz)
Phase Noise (156.250 MHz):	-67dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -112dBc/Hz @ 1kHz -121dBc/Hz @ 10kHz, -124dBc/Hz @ 100kHz, -136dBc/Hz @ 1MHz, -153dBc/Hz @ 5MHz
Aging:	< ±2ppm max. for the first year; ±10ppm max.over 10 years
Reflow Condition:	260°C max for 10 sec.

GERMANY:

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