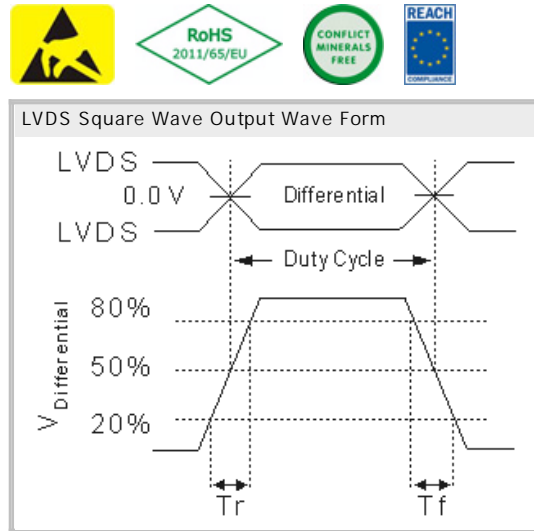
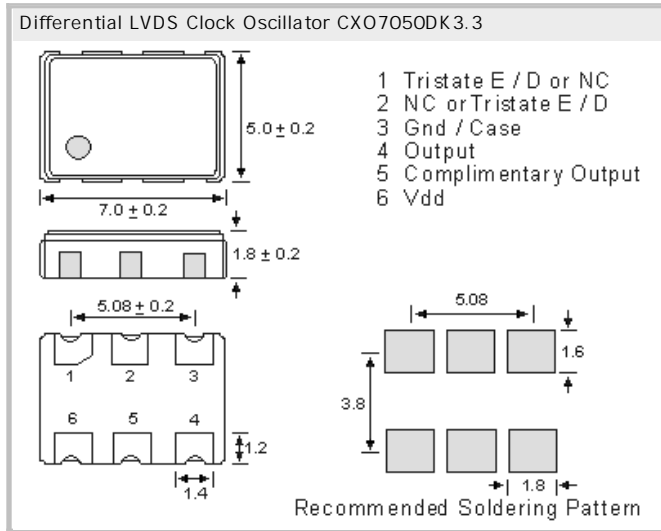


Differential LVDS Clock Oscillator  
CXO7050DK3.3, 3.3V, 0.2ps Jitter

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- Femto second integrated phase jitter (0.2ps typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -142 dBc/Hz at 100 KHz offset)
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave



## Specifications

Holder Type:	Differential LVDS Clock Oscillator CXO7050DK3.3; 3.3V; Tri-State on pad 1
Frequency Range:	13.500 MHz ~ 200.000 MHz
Frequency Stability at 25°C:	± 20 to ± 100 ppm
Operating Temperature Range:	-20° C to + 70° C, -40° C to + 85° C
Storage Temperature:	-50° C to + 100° C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 5%
Maximum Supply Current (15pF load):	16mA typica; 27mA max.
Output Swing:	350 mV min. ( Vdd = + 2.5V )
Output Logic Levels:	High "1" 1.43V typical; 1.6V max, RL= 100 ohms.; Low "0" 0.9V min; 1.1V typical, RL= 100 ohms
Output Symmetry (Duty Cycle):	50% ± 5% max. measured at 50% waveform
Load:	RL= 100 between output and complimentary output
Rise/Fall Time:	Tr = 0.2 ns. typ; 0.4 ns. max. 20% -> 80% of waveform Tf = 0.2 ns. typ; 0.4 ns. max. 80% -> 20% of waveform
Start Up Time:	5.0 ms typical; 10.0 ms typical;
Tri-state Function Pin 1:	If no connection or Vdd * 70% min is applied: Output. Internal pull-up Oscillation disable time is 2µs max. If Vdd* 30% max is applied: High impedance. 10µA typ., enable time 2ms max.
Phase Jitter (12 kHz to 20 MHz):	0.2 ps typical, 0.5 ps (max.)
Phase Noise (125 MHz):	-60dBc/Hz @ 10Hz, -90dBc/Hz @ 100Hz, -120dBc/Hz @ 1kHz -136dBc/Hz @ 10kHz, -142dBc/Hz @ 100kHz, -145dBc/Hz @ 1MHz, -148dBc/Hz @ 10MHz
Aging:	< ± 3ppm max. for the first year
Reflow Condition:	260° C max for 10 sec.

### GERMANY:

COMTEC CRYSTALS GmbH · Sultenstrasse 12-14  
8 5 5 8 6 P o i n g / G E R M A N Y  
Phone +49 8121 778160 · Fax +49 8121 778177  
e-Mail [info@comtec-crystals.com](mailto:info@comtec-crystals.com)  
Internet: <http://www.comtec-crystals.com>  
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### FRANCE:

COMTEC CRYSTALS SARL · 23, rue du Faucon  
6 7 5 0 0 H a g u e n a u / F R A N C E  
Phone + 33 388 732162 · Fax + 33 388 730118  
e-Mail [sales@comtec-crystals.com](mailto:sales@comtec-crystals.com)  
Internet: <http://www.comtec-crystals.com>  
Sous réserve de modifications.