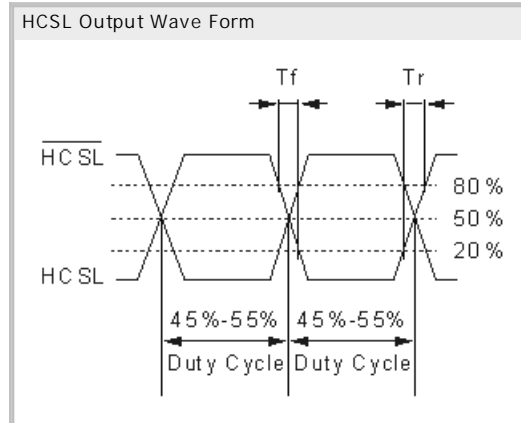
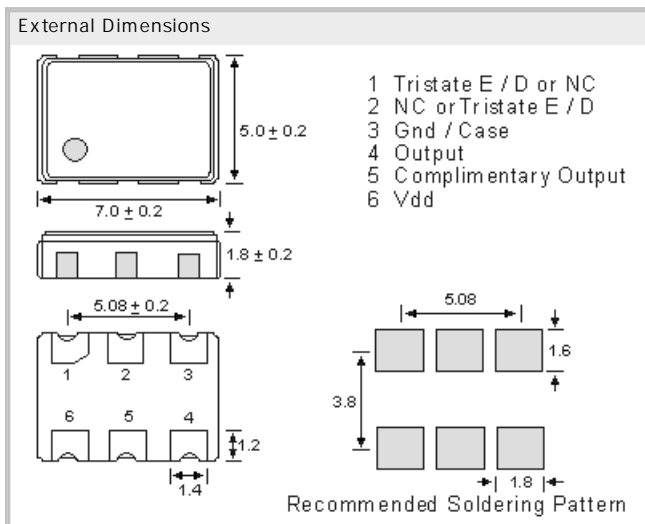


Differential HCSSL Clock Oscillator, no PLL
CXO7050CK 3.3, 3.3V, 200 fsec Jitter

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- Fem to second integrated phase jitter (200 fs typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -144 dBc/Hz at 100 KHz offset)
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- High performance with surprisingly low price



Specifications - Product No. G056448000QARUPN43CB

Holder Type:	CXO7050CK 3.3; 3.3V(Voltage code is "3.3"); Tri-State on pad 1
Frequency:	56.448000 MHz
Frequency Stability at 25°C:	± 100 ppm
Operating Temperature Range:	± 100 ppm over -40°C to +85°C (inclusive of 25°C tolerance, ± 10% input voltage variation, load change, aging, shock and vibration)
Storage Temperature:	-55°C to +125°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 10%
Maximum Supply Current (15pF load):	17.0mA typ.
Output Swing:	620 mV min; 700 mV typical; 780 mV max.
Output Logic Levels:	High "1" Voh 660 mV min.; 740 mV typical; 850 mV max. Low "0" Vol -150 mV min.; 0 mV typical; 150 mV max.
Output Symmetry (Duty Cycle):	50% ± 5% max. measured at Q and complimentary Q cross point
Load:	RL= 50 Ohm to ground on each output
Rise/Fall Time:	0.15 ns. typ; 0.4 ns. max. 20% -> 80% of HCSSL waveform/(RL = 100 , CL = 10pF)
Start Up Time:	3 ms typical; 10 ms max.
OE Function:	-Enable: When 70% min. of VDD to Enable Output. Enable time: 10ms -Disable: When 30% max. of VDD to Disable Output. Disable current : 10 µA, Disable time : 0,2 µs (max.)
Phase Jitter (12 kHz to 20 MHz):	0,2ps typical; for 155,520 MHz
Phase Noise (125 MHz):	-50dBc/Hz @ 10Hz, -82dBc/Hz @ 100Hz, -116dBc/Hz @ 1kHz -138dBc/Hz @ 10kHz, -144dBc/Hz @ 100kHz, -149dBc/Hz @ 1MHz, -155dBc/Hz @ 10MHz
Aging:	< ± 3ppm max. for the first year; ± 2ppm max. per year thereafter
Reflow Condition:	260°C max for 10 sec.

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