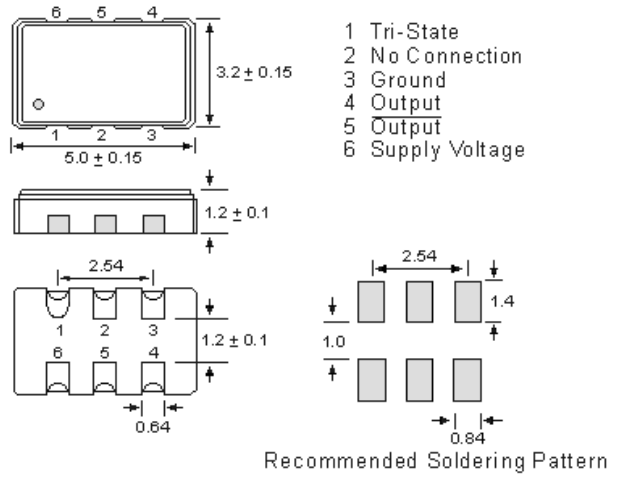
COMTEC CRYSTALS Group Data Sheet

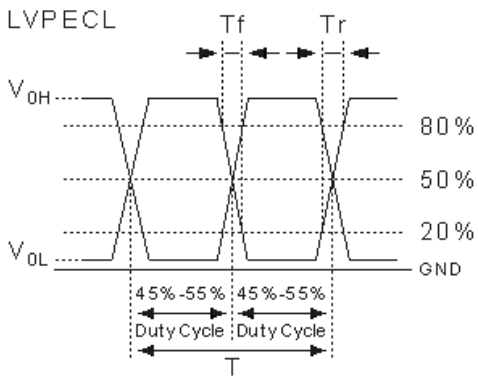
Clock Oscillator Differential CXP5032PQF2.5
LVPECL 2.5V; ultra low jitter, with PLL

- SMD in ceramic case (5.0 x 3.2 x 1.2) mm
- Tri-State Enable / Disable on pad No. 1
- LVPECL Differential Output Wave Form
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies

Clock Oscillator Differential CXP5032PQF2.5



LVPECL Square Wave Output Wave Form



Specifications

Holder Type:	CXP5032PQF2.5 ; 2.5V(Voltage code is "2.5); Tri-State on pad 1
Frequency Range:	10 MHz to 1450.0 MHz
Frequency Stability at 25°C:	±25 ppm / ±50 ppm
Operating Temperature Range:	±25 ppm, -40°C to +85°C / ±50 ppm, -40°C to +85°C
Storage Temperature:	-55°C to +125°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 10%
Maximum Supply Current (Differential):	68mA max.
Current with Output:	16 mA typical
Output Voltage (VOH) (VOL):	High "1" Vdd-1.03V min, Vdd- 0.6Vmax. Low "0" Vdd-1.85V min, Vdd- 1.6Vmax.
Start Up Time:	10 ms max.
Output Symmetry (Duty Cycle):	50% ± 2%max. (measured at 50% Vdd)
Load:	Differential
Rise (Tr) /Fall Time (Tf):	0.2ns typical; 0.5ns max. (10%Vdd<->90%Vdd, 15pF load)
OE Function Pin 1:	-Enable: When 70% min. of VDD to Enable Output.(Open connection prohibit.) -Disable:When 30% max. of VDD to Disable Output. (high impedance).
Ouput Enable Time / Disable Time:	200 nS. Max. / 50 nS. Max.
Phase Jitter:	1.0ps typ. (12 kHz to 20 MHz); < 100 fs (1.875 MHz to 20MHz)
Phase Noise (156.250 MHz):	-67dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -112dBc/Hz @ 1kHz -121dBc/Hz @ 10kHz, -124dBc/Hz @ 100kHz, -136dBc/Hz @ 1MHz, -153dBc/Hz @ 5MHz
Aging:	< ±2ppm max. for the first year; ±10ppm max.over 10 years
Reflow Condition:	260°C max for 10 sec.

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